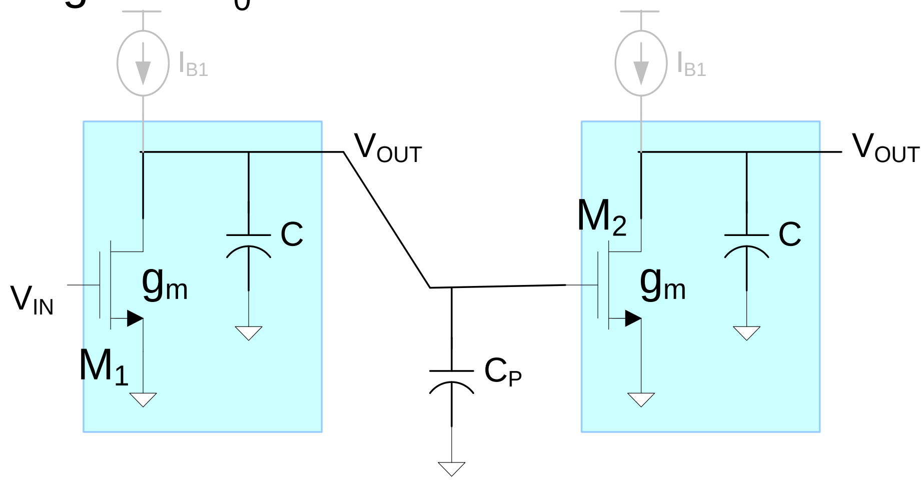
EE 508 Lecture 35

High Frequency Filters

Review from last lecture

Single-ended High-Frequency TA Integrators

How high can I_0 be?



$$I_{0M} = \frac{\mu V_{EB1}}{L_{min}^2}$$

$$I_{0M} = \omega_T$$

(neglected C and C_P)

Speed of operation increases with V_{EB}

V_{EB} is limited by signal swing requirements and V_{DD}

Signal Swing:

$$V_{DD} - V_T - V_{EB} = V_T + V_{EB} - (V_T + 100mV)$$

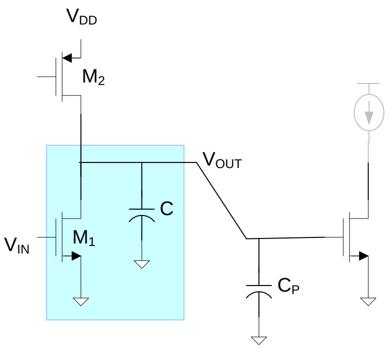
$$V_{EB} = \frac{V_{DD} + 100mV - V_T}{2}$$

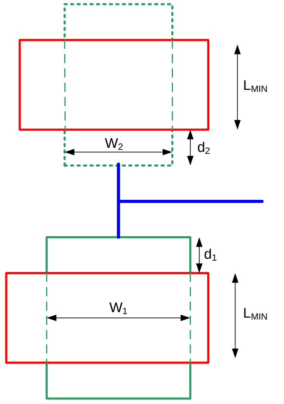
$$I_{OMAX} \cong \frac{\mu\left(V_{DD} + 100mV - V_T\right)}{2L_{min}^2}$$

Review from last lecture

How high can I_0 be?

Consider a basic layout





$$I_0 = \frac{\omega_T}{1+\left(3h_{BOT}\left[1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+h_{SW}\left[12\frac{\lambda}{W_1}+1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

Example: Consider the 0.25u TSMC CMOS Process

$$I_0 = \frac{\omega_T}{1+\left(3\bullet 0.31\left[1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+0.61\left[12\frac{0.125}{W_1}+1+4.01\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

$$h_{BOT} = 0.31$$

$$h_{SW} = 0.61$$

$$I_0 = \frac{\omega_T}{1+\left(0.931\left[1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+0.61\left[\frac{1.5}{W_1}+1+4.01\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

$$\frac{\mu_n}{\mu_p} = 4.1$$

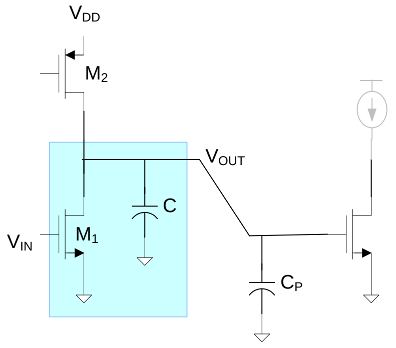
GATE term

BOT term

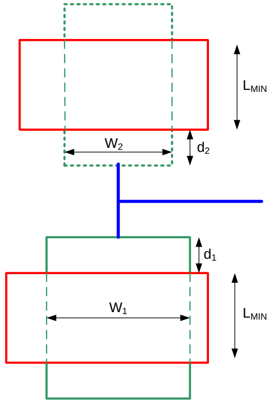
SW term

Review from last lecture

How high can I_0 be?



Consider a basic layout



Example: Consider the 0.25u TSMC CMOS Process

$$I_0 = \frac{\omega_T}{1+\left(0.93\left[1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+0.61\left[\frac{1.5}{W_1}+1+4.01\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

GATE term

BOT term

SW term

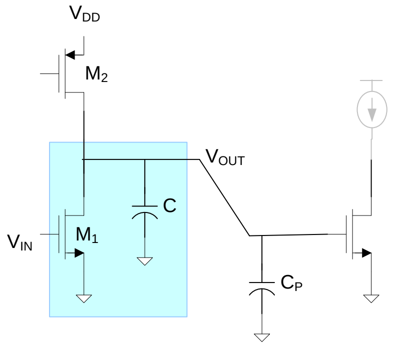
If W_1=1.5u and $V_{EB1}=V_{EB2}$

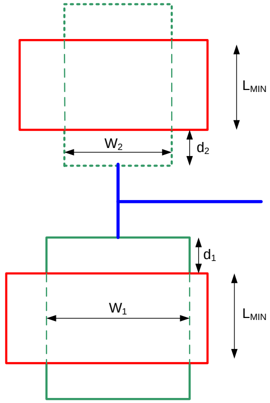
$$I_0 = \frac{\omega_T}{1+(4.73+4.03)} = .102\omega_T$$

- The diffusion capacitance term can dominate the C_{GS} term
- The SW capacitance can be the biggest contributor to the speed limitations
- A factor of 10 or even much more reduction in speed is possible due to the diffusion parasitics and layout
- Maximizing W_1 will minimize I_0 but power will get very large for marginal improvement in speed

How high can I_0 be?

Consider a basic layout





Example: Consider the 0.25u TSMC CMOS Process

$$I_0 = \frac{\omega_T}{1+\left(0.93\left[1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+0.61\left[\frac{1.5}{W_1}+1+4.01\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

BOT term (the $0.93[\ldots]$ term)

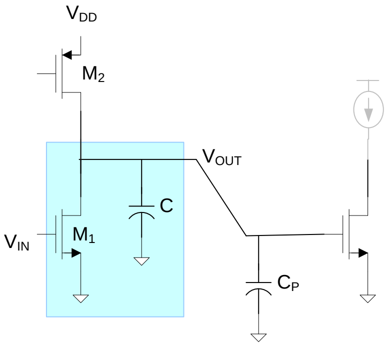
SW term (the $0.61[\ldots]$ term)

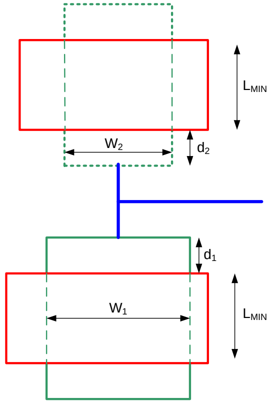
This example shows that layout is really critical when high speed operation is needed

What can be done with layout to improve performance?

How high can I_0 be?

Consider a basic layout

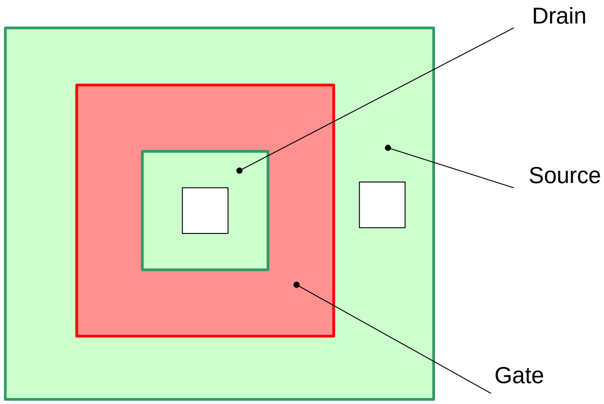


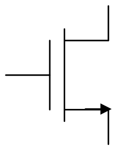


What can be done with layout to improve performance?

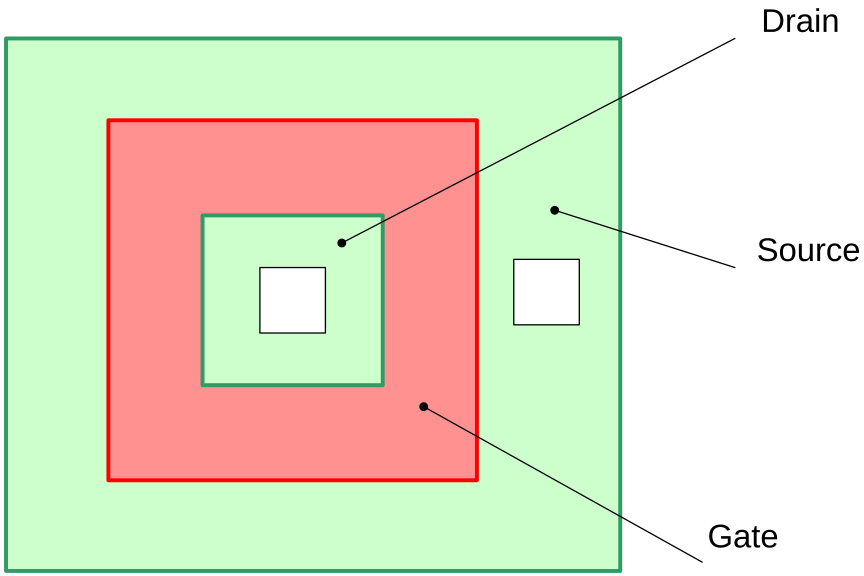
Reducing the diffusion capacitances on the drains will have a major impact on speed!

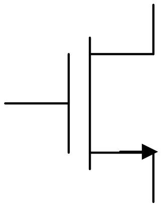
Consider a concentric layout approach:





Concentric Layouts





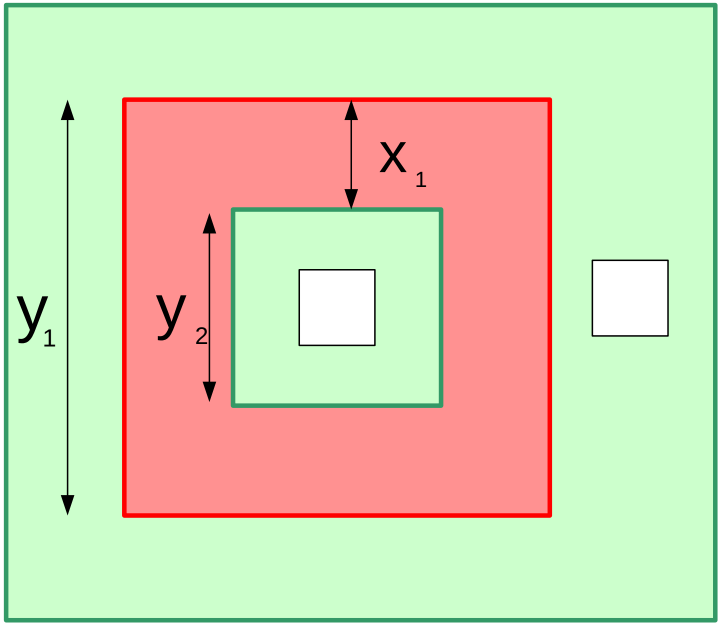
Can be shown this is equivalent to a rectangular transistor (W_{EQ}/L_{EQ})

Drain area and perimeter dramatically reduced

Source area and perimeter dramatically increased (but does not degrade performance)

Only sidewall is adjacent to the gate and C_{SW} is usually considerably lower here though some models do not provide separate characterization

Concentric Layouts



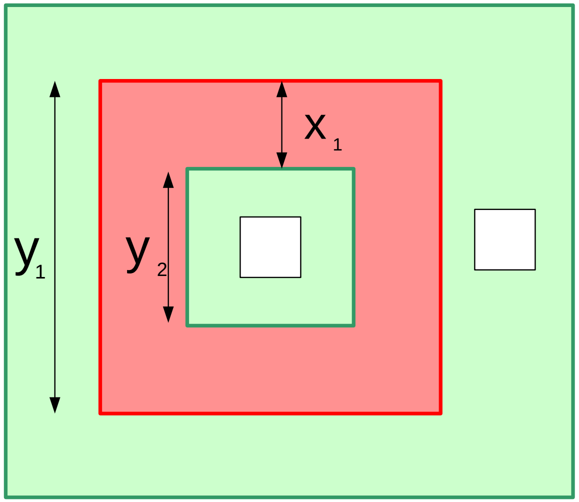
$$W_{EQ} \cong 4\left(\frac{y_1+y_2}{2}\right) \quad \text{or} \quad W_{EQ} \cong 4\left(y_2 + \sqrt{2}\left[\frac{y_1 - y_2}{4}\right]\right)$$

$$L_{EQ} \cong x_1$$

Exact closed-form expressions exist which are somewhat more complicated

How high can I_0 be?

Consider concentric layouts for M_1 and M_2



Recall $$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2$$

Assume $W_2 > W_1$

Will minimize the diffusion capacitance by starting with a minimum-sized concentric device

Thus $y_2 = 6\lambda$ $\quad X_1 = 2\lambda$ $\quad y_1 = 10\lambda$ $\quad W_{1min} \cong 4\lambda\left(6+\sqrt{2}\right)$

Define K_1 to be the scaling factor of W_1 above that of the minimum-sized concentric device

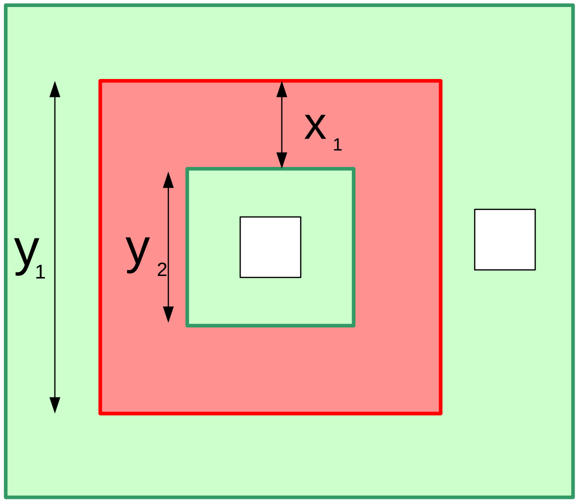
$$K_1 = \frac{W_1}{W_{1min}}$$

Assume, for convenience, that K is an integer

M_1 realized by placing K_1 minimum-sized concentric devices in parallel

How high can I_0 be?

Consider concentric layouts for M_1 and M_2



$y_2=6\lambda$ $x_2=2\lambda$ $y_1=10\lambda$

$$W_{1min} \cong 4\lambda\left(6+\sqrt{2}\right)$$

$$K_1 = \frac{W_1}{W_{1min}}$$

Consider now the concentric layout for M_1

$P_{D1}=K_1 24\lambda$ $A_{D1}=K_1(6\lambda)^2$ $A_{GATE1}=K_1(48\lambda^2+16\lambda^2)$

Consider now the concentric layout for M_2

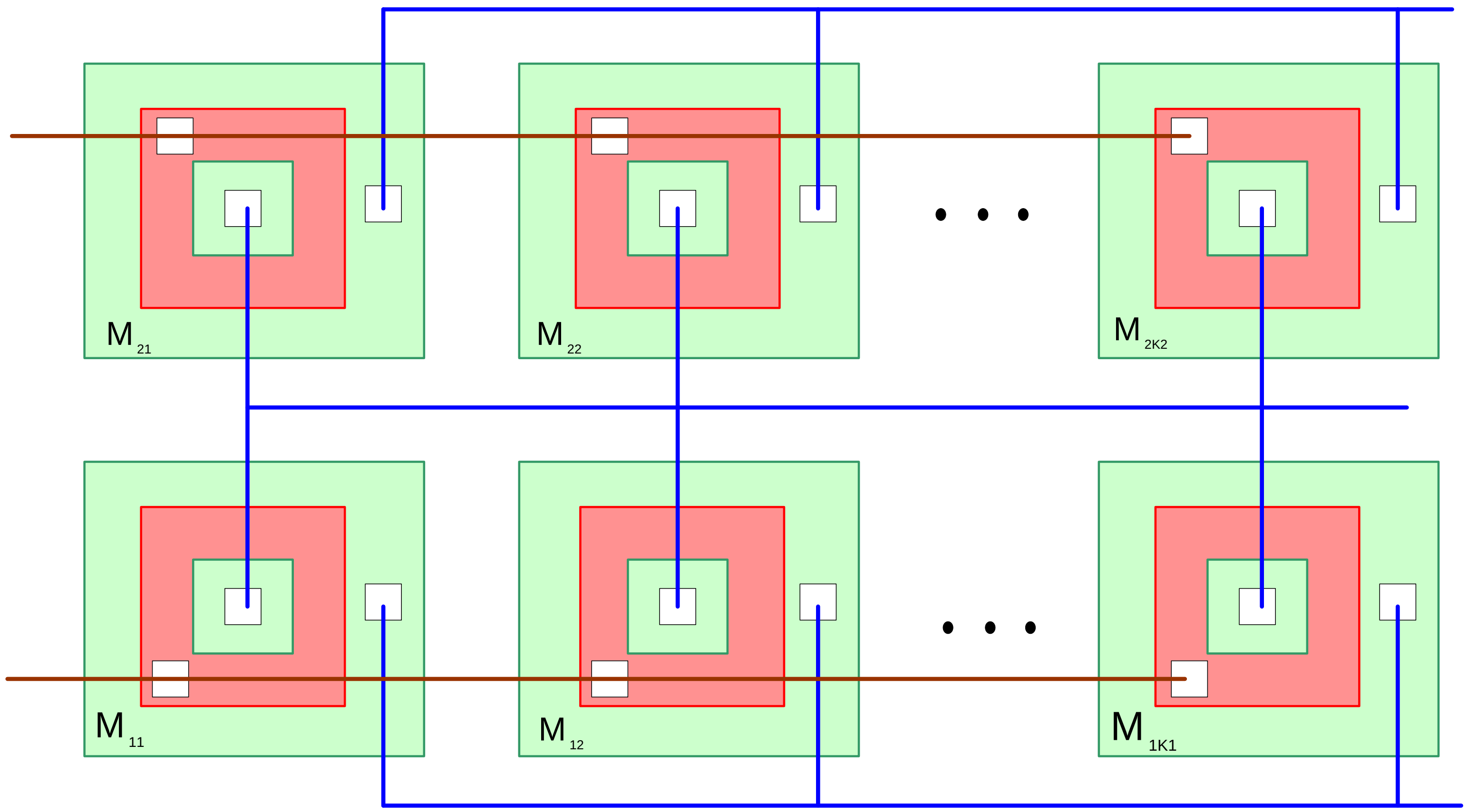
The minimum-sized layout (gate,source, and drain) for the p-channel transistors are identical to those for n-channel transistors

Define K_2 to be the scaling factor for W_2 above that of a minimum-sized concentric device

$P_{D2}=K_2 24\lambda$ $A_{D2}=K_2(6\lambda)^2$

How high can I_0 be?

Consider concentric layouts for M_1 and M_2

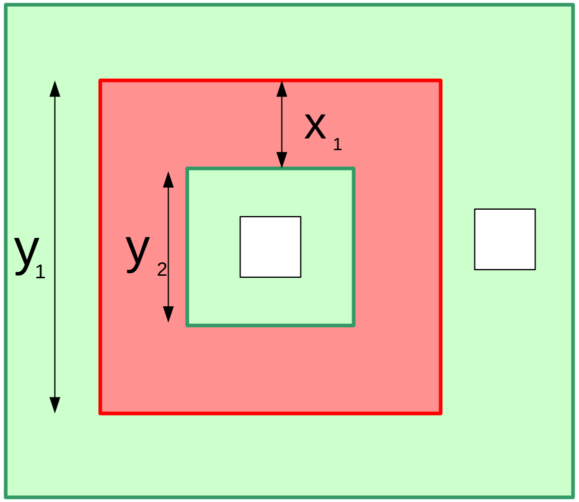


Individual segments can be a little bigger than minimum sized w/o major change in performance

May select K_1=K_2=1

How high can I_0 be?

Consider concentric layouts for M_1 and M_2



$$K_2 = \frac{W_2}{W_{1min}} \qquad W_2 = W_1 \frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2$$

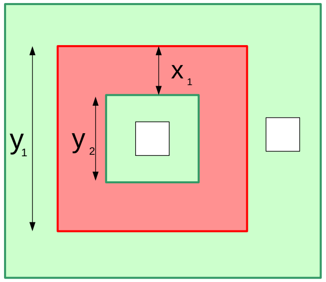
$$K_2 = \frac{W_1}{W_{1min}} \frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2 = K_1 \frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)$$

$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{L_{min}\left(C_{P1} + C_{P2}\right) + C_{OX} W_1 L_{min}^2} \quad \Rightarrow \quad I_0 = \frac{\dfrac{\mu C_{OX} W_1 V_{EB1}}{L_{min}}}{\left(C_{P1} + C_{P2}\right) + C_{GS1}}$$

$$I_0 = \frac{\dfrac{\mu V_{EB1}}{L_{min}^2}}{\dfrac{\left(C_{P1} + C_{P2}\right) + C_{GS1}}{C_{OX} L_{min} W_1}} \qquad I_0 = \frac{\omega_T}{\dfrac{\left(C_{P1} + C_{P2}\right) + C_{GS1}}{2\lambda C_{OX} W_1}}$$

How high can I_0 be?

Consider concentric layouts for M_1 and M_2



$$I_0 = \frac{\omega_T}{\dfrac{\left(C_{P1}+C_{P2}\right)+C_{GS1}}{2\lambda C_{OX} W_1}}$$

$P_{D1}=K_1 24\lambda$ $\quad A_{D1}=K_1(6\lambda)^2$ $\quad A_{GATE1}=K_1(48\lambda^2+16\lambda^2)$

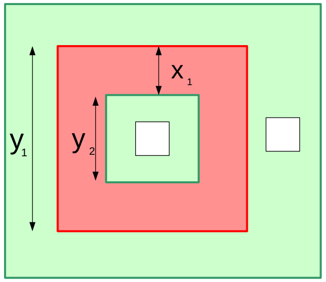
$P_{D2}=K_2 24\lambda$ $\quad A_{D2}=K_2(6\lambda)^2$ $\quad W_1 \cong 4K_1\lambda\left(6+\sqrt{2}\right)$

$$I_0 = \frac{\omega_T}{\dfrac{C_{OX}K_1\left(48\lambda^2+16\lambda^2\right)+\left(C_{SWn}K_1 24\lambda+C_{BOTn}K_1\left(6\lambda\right)^2+C_{SWp}K_2 24\lambda+C_{BOTp}K_2\left(6\lambda\right)^2\right)}{2\lambda C_{OX}4K_1\lambda\left(6+\sqrt{2}\right)}}$$

$$I_0 = \frac{\omega_T}{\dfrac{C_{OX}K_1\left(48\lambda^2+16\lambda^2\right)+C_{BOT}\left(6\lambda\right)^2\left(K_1+K_2\right)+C_{SW}24\lambda\left(K_1+K_2\right)}{2\lambda C_{OX}4K_1\lambda\left(6+\sqrt{2}\right)}}$$

How high can I_0 be?

Consider concentric layouts for M_1 and M_2



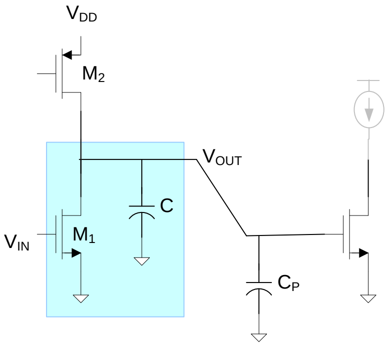
$$I_0 = \frac{\omega_T}{\dfrac{C_{OX}K_1\left(48\lambda^2+16\lambda^2\right)+C_{BOT}(6\lambda)^2(K_1+K_2)+C_{SW}24\lambda(K_1+K_2)}{2\lambda C_{OX}4K_1\lambda\left(6+\sqrt{2}\right)}}$$

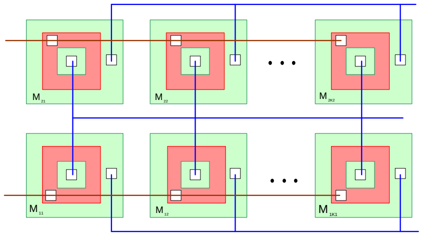
$$I_0 = \frac{\omega_T}{\dfrac{(8)+h_{BOT}4.5(1+K_2/K_1)+h_{SW}3(1+K_2/K_1)}{\left(6+\sqrt{2}\right)}}$$

$$I_0 = \frac{\omega_T}{1.08+h_{BOT}.61(1+K_2/K_1)+h_{SW}0.4(1+K_2/K_1)}$$

How high can I_0 be?

Consider concentric layout





$$I_0 = \frac{\omega_T}{1.08 + h_{BOT}.61(1+K_2/K_1) + h_{SW}0.4(1+K_2/K_1)}$$

Example: Consider the 0.25u TSMC CMOS Process with W_1=1.5u and V_{EB1}=V_{EB2}

$$\frac{K_2}{K_1} = \frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right) \qquad \frac{K_2}{K_1} = 4.01\left(\frac{V_{EB1}}{V_{EB2}}\right) \qquad \frac{\mu_n}{\mu_p} = 4.1$$

$$I_0 = \frac{\omega_T}{1.08 + .19(5.01) + 0.24(5.01)}$$

BOT term SW term

$$I_0 = \frac{\omega_T}{1.08 + .95 + 1.2}$$

$$I_0 = .31\omega_T$$

Diffusion parasitics still dominate frequency degradation

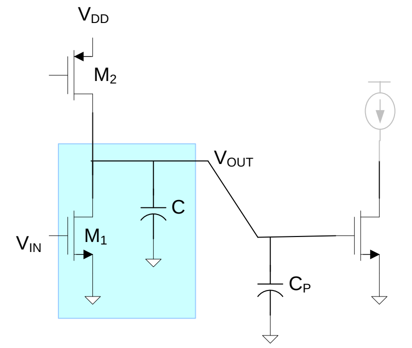
SW term probably over-estimated since it is an internal SW capacitance

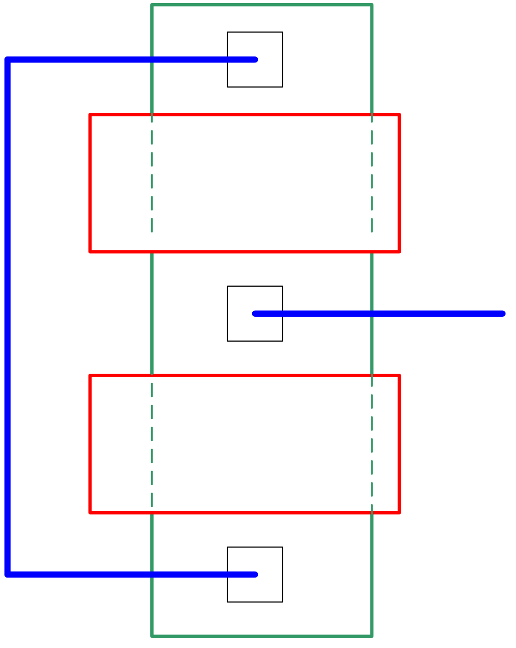
But a factor of 3 faster with the concentric layout compared to standard layout

How high can I_0 be?

Other layouts for enhancing speed of operation

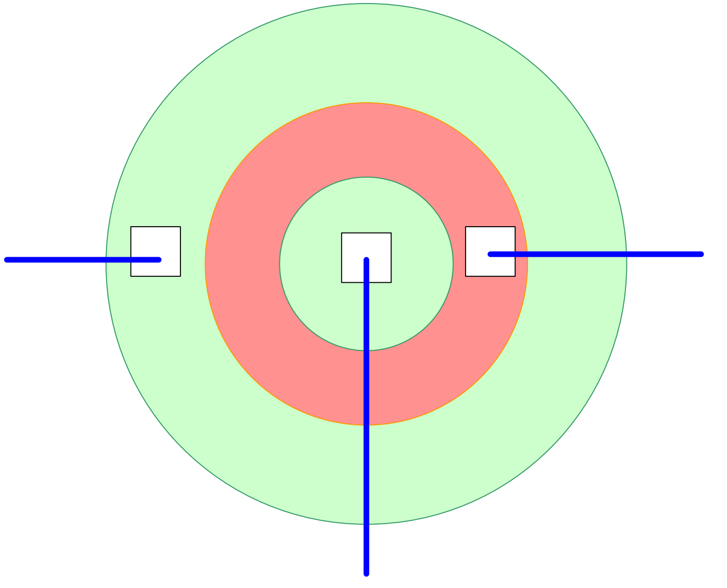
Goal: reduce area and perimeter on drain





Shared-drain structure

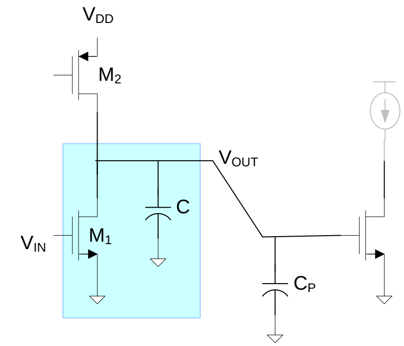
(but would not be applicable if one device in well and one outside of well)



Circular-concentric structure

Though the reduced size drain structures work very well, CAD support may be limited for layout, simulation, and extraction

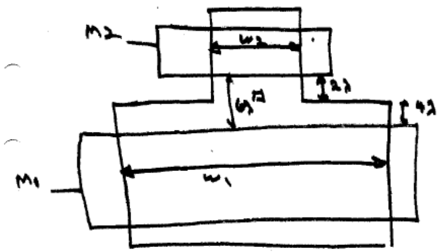
How high can I_0 be?



Other layouts for enhancing speed of operation

Goal: reduce area and perimeter on drain

n-channel load, simple Layout $\quad W_1 = 4W_2$



(but would not be applicable if one device in well and one outside of well)

$$A_D = 4\lambda W_1 + 2\lambda W_2 = 18\lambda W_2$$

$$P_D = 12\lambda + 2W_1 = 12\lambda + 8W_2$$

$$A_{G1} = 2\lambda W_1 = 8\lambda W_2$$

$$A_{G2} = 2\lambda W_2$$

$$\tilde{\omega}_0 = \frac{\sqrt{3}}{2}\frac{g_{m1}}{C_L}$$

$$\tilde{\omega}_0 = \frac{\frac{\sqrt{3}}{2}\frac{\mu_n V_{EB1}}{4\lambda^2}}{\frac{5}{4} + \frac{9}{4}h_{bot} + \left(1 + \frac{1}{4K}\right)h_{sw}} \qquad K = \frac{W_2}{6\lambda}$$

Useful for adding loss or in high-speed gain stages

(can add loss with n-channel or p-channel device)

Parameters from .25u TSMC Process

u	3.74E+10	1/(V*sec)
2*lambda	0.25	u
hsw	0.61	none
ot	0.32	none
/up	4.1	

Integrator Io for Special Layouts

file: integrator-speed-comp

Note: Process parameters may be a little optimistic but relative performance should be as predicted

Conventional Layout

VEB1/ VEB2	K	W1	W2	SWn	SWp	BOTn	BOTp	SW comp Total	Bot comp Total	Load comp	Den	VEB1	Io,no diff GHz	Io GHz
1	1	0.75	3.075	0.92	3.42	0.96	3.94	4.33	4.90	1	10.2	1	95.3	9.3
1	2	1.5	6.15	0.61	3.11	0.96	3.94	3.72	4.90	1	9.6	1	95.3	9.9
1	4	3	12.3	0.46	2.96	0.96	3.94	3.42	4.90	1	9.3	1	95.3	10.2
1	8	6	24.6	0.38	2.88	0.96	3.94	3.26	4.90	1	9.2	1	95.3	10.4
1	16	12	49.2	0.34	2.84	0.96	3.94	3.19	4.90	1	9.1	1	95.3	10.5
0.5	1	0.75	0.769	0.92	1.54	0.96	0.98	2.46	1.94	1	5.4	1	95.3	17.6
0.5	2	1.5	1.538	0.61	1.24	0.96	0.98	1.85	1.94	1	4.8	1	95.3	19.9
0.5	4	3	3.075	0.46	1.08	0.96	0.98	1.54	1.94	1	4.5	1	95.3	21.2
0.5	8	6	6.15	0.38	1.01	0.96	0.98	1.39	1.94	1	4.3	1	95.3	22.0
0.5	16	12	12.3	0.34	0.97	0.96	0.98	1.31	1.94	1	4.3	1	95.3	22.4
2	1	0.75	12.3	0.92	10.92	0.96	15.74	11.83	16.70	1	29.5	1	95.3	3.2
2	2	1.5	24.6	0.61	10.61	0.96	15.74	11.22	16.70	1	28.9	1	95.3	3.3
2	4	3	49.2	0.46	10.46	0.96	15.74	10.92	16.70	1	28.6	1	95.3	3.3
2	8	6	98.4	0.38	10.39	0.96	15.74	10.77	16.70	1	28.5	1	95.3	3.3
2	16	12	196.8	0.34	10.35	0.96	15.74	10.69	16.70	1	28.4	1	95.3	3.4
1	1	0.75	3.075	0.92	3.42	0.96	3.94	4.33	4.90	1	10.2	1.5	142.9	14.0
1	2	1.5	6.15	0.61	3.11	0.96	3.94	3.72	4.90	1	9.6	1.5	142.9	14.9
1	4	3	12.3	0.46	2.96	0.96	3.94	3.42	4.90	1	9.3	1.5	142.9	15.3
1	8	6	24.6	0.38	2.88	0.96	3.94	3.26	4.90	1	9.2	1.5	142.9	15.6
1	16	12	49.2	0.34	2.84	0.96	3.94	3.19	4.90	1	9.1	1.5	142.9	15.7
0.5	1	0.75	0.769	0.92	1.54	0.96	0.98	2.46	1.94	1	5.4	1.5	142.9	26.5
0.5	2	1.5	1.538	0.61	1.24	0.96	0.98	1.85	1.94	1	4.8	1.5	142.9	29.8
0.5	4	3	3.075	0.46	1.08	0.96	0.98	1.54	1.94	1	4.5	1.5	142.9	31.9
0.5	8	6	6.15	0.38	1.01	0.96	0.98	1.39	1.94	1	4.3	1.5	142.9	33.0
0.5	16	12	12.3	0.34	0.97	0.96	0.98	1.31	1.94	1	4.3	1.5	142.9	33.6
2	1	0.75	12.3	0.92	10.92	0.96	15.74	11.83	16.70	1	29.5	1.5	142.9	4.8
2	2	1.5	24.6	0.61	10.61	0.96	15.74	11.22	16.70	1	28.9	1.5	142.9	4.9
2	4	3	49.2	0.46	10.46	0.96	15.74	10.92	16.70	1	28.6	1.5	142.9	5.0
2	8	6	98.4	0.38	10.39	0.96	15.74	10.77	16.70	1	28.5	1.5	142.9	5.0
2	16	12	196.8	0.34	10.35	0.96	15.74	10.69	16.70	1	28.4	1.5	142.9	5.0
1	1	0.75	3.075	0.92	3.42	0.96	3.94	4.33	4.90	1	10.2	2	190.6	18.6
1	2	1.5	6.15	0.61	3.11	0.96	3.94	3.72	4.90	1	9.6	2	190.6	19.8
1	4	3	12.3	0.46	2.96	0.96	3.94	3.42	4.90	1	9.3	2	190.6	20.5
1	8	6	24.6	0.38	2.88	0.96	3.94	3.26	4.90	1	9.2	2	190.6	20.8
1	16	12	49.2	0.34	2.84	0.96	3.94	3.19	4.90	1	9.1	2	190.6	21.0
0.5	1	0.75	0.769	0.92	1.54	0.96	0.98	2.46	1.94	1	5.4	2	190.6	35.3
0.5	2	1.5	1.538	0.61	1.24	0.96	0.98	1.85	1.94	1	4.8	2	190.6	[illegible]
0.5	4	3	3.075	0.46	1.08	0.96	0.98	1.54	1.94	1	4.5	2	[illegible]	42.5
0.5	8	6	6.15	0.38	1.01	0.96	0.98	1.39	1.94	1	4.3	2	190.6	44.0
0.5	16	12	12.3	0.34	0.97	0.96	0.98	1.31	1.94	1	4.3	2	190.6	44.8
2	1	0.75	12.3	0.92	10.92	0.96	15.74	11.83	16.70	1	29.5	2	190.6	6.5
2	2	1.5	24.6	0.61	10.61	0.96	15.74	11.22	16.70	1	28.9	2	190.6	[illegible]
2	4	3	49.2	0.46	10.46	0.96	15.74	10.92	16.70	1	28.6	2	190.6	6.7
2	8	6	98.4	0.38	10.39	0.96	15.74	10.77	16.70	1	28.5	2	190.6	6.7
2	16	12	196.8	0.34	10.35	0.96	15.74	10.69	16.70	1	28.4	2	190.6	6.7

Note: Significant change in speed with optimal choice of design variables

Parameters from .25u TSMC Process

u	3.74E+10	1/(V*sec)
2*lambda	0.25	u
hsw	0.61	none
hbot	0.32	none
µn/up	4.1	

Integrator Io for Special Layouts

file: integrator-speed-comp

Note: Process parameters may be a little optimistic but relative performance should be as predicted

Concentric Layout

VEB1/ VEB2	K	K2	K2^	W1	W2	SWn	SWp	BOTn	BOTp	SW comp Total	Bot comp Total	Load Comp	Den	VEB1	Io,no dif GHz	Io GHz
1	1	4.8		3.7	15.2	0.25	1.19	0.19	4.53	1.44	4.73	1.08	7.24	1	88.3	13.2
1	2	8.9		6.7	27.5	0.27	1.22	0.43	8.56	1.49	8.99	1.04	11.53	1	91.3	8.3
1	4	17.1		12.7	52.1	0.29	1.23	0.91	16.63	1.52	17.53	1.02	20.08	1	93.1	4.7
1	1	4.8		3.7	15.2	0.25	1.19	0.19	4.53	1.44	4.73	1.08	7.24	1.5	132.5	19.7
1	2	8.9		6.7	27.5	0.27	1.22	0.43	8.56	1.48	8.99	1.04	11.53	1.5	136.9	12.4
1	4	17.1		12.7	52.1	0.29	1.23	0.91	16.63	1.52	17.53	1.02	20.08	1.5	139.7	7.1
1	1	4.8		3.7	15.2	0.25	1.19	0.19	4.53	1.44	4.73	1.08	7.24	2	176.6	26.3
1	2	8.9		6.7	27.5	0.27	1.22	0.43	8.56	1.49	6.99	1.04	11.53	2	182.6	16.5
1	4	17.1		12.7	52.1	0.29	1.23	0.91	16.63	1.52	17.53	1.02	20.08	2	186.3	9.5
0.5	1	1.0		3.7	3.8	0.25	0.25	0.19	0.21	0.50	0.40	1.08	1.98	1	88.3	48.1
0.5	2	2.1		6.7	6.9	0.27	0.28	0.43	0.45	0.55	0.88	1.04	2.48	1	91.3	38.4
0.5	4	4.1		12.7	13.0	0.29	0.30	0.91	0.96	0.58	1.86	1.02	3.47	1	93.1	27.5
0.5	1	1.0		3.7	3.8	0.25	0.25	0.19	0.21	0.50	0.40	1.08	1.98	1.5	132.5	72.2
0.5	2	2.1		6.7	6.9	0.27	0.28	0.43	0.45	0.55	0.88	1.04	2.48	1.5	136.9	[illegible]
0.5	4	4.1		12.7	13.0	0.29	0.30	0.91	0.96	0.58	1.86	1.02	3.47	1.5	139.[illegible]	41.2
0.5	1	1.0		3.7	3.8	0.25	0.25	0.19	0.21	0.50	0.40	1.08	1.98	2	17[illegible].6	96.2
0.5	2	2.1		6.7	6.9	0.27	0.28	0.43	0.45	0.55	0.88	1.04	2.48	2	1[illegible]2.6	76.8
0.5	4	4.1		12.7	13.0	0.29	0.30	0.91	0.96	0.58	1.86	1.02	3.47	2	18[illegible].3	54.9
2	1	20.0		3.7	60.8	0.25	4.94	0.19	77.92	5.19	78.11	1.08	84.38	1	88.3	1.1
2	2	36.4		6.7	110.0	0.27	4.97	0.43	142.47	5.24	142.90	1.04	149.18	1	9[illegible].3	0.6
2	4	69.2		12.7	208.4	0.29	4.99	0.91	271.56	5.27	272.47	1.02	278.77	1	9[illegible].1	0.3
2	1	20.0		3.7	60.8	0.25	4.94	0.19	77.92	5.19	78.11	1.08	84.38	1.5	13[illegible].5	1.7
2	2	36.4		6.7	110.0	0.27	4.97	0.43	142.47	5.24	142.90	1.04	149.18	1.5	136.[illegible]	1.0
2	4	69.2		12.7	208.4	0.29	4.99	0.91	271.56	5.27	272.47	1.02	278.77	1.5	139.7	[illegible]
2	1	20.0		3.7	60.8	0.25	4.94	0.19	77.92	5.19	78.11	1.08	84.38	2	176.6	2.3
2	2	35.4		6.7	110.0	0.27	4.97	0.43	142.47	5.24	142.90	1.04	149.18	2	182.6	1.3
2	4	69.2		12.7	208.4	0.29	4.99	0.91	271.56	5.27	272.47	1.02	278.77	2	186.3	0.7

Segmented Conccentric Layout

VEB1/ VEB2	K	K2	K2^	W1	W2	SWn	SWp	BOTn	BOTp	SW comp Total	Bot comp Total	Load Comp	Den	VEB1	Io,no dif GHz	Io GHz
1	1	4.8	2.3	3.71	15.2	0.25	1.13	0.19	2.05	1.38	2.24	1.08	4.70	1	88.3	20.3
1	2	8.9	4.35	6.71	27.5	0.27	1.19	0.43	4.06	1.46	4.49	1.04	6.99	1	91.3	13.6
1	4	17.1	8.45	12.71	52.1	0.29	1.22	0.91	8.09	1.50	8.99	1.02	11.52	1	93.1	8.3
1	1	4.8	2.3	3.71	15.2	0.25	1.13	0.19	2.05	1.38	2.24	1.08	4.70	1.5	132.5	30.4
1	2	8.9	4.35	6.71	27.5	0.27	1.19	0.43	4.06	1.46	4.49	1.04	6.99	1.5	136.9	20.4
1	4	17.1	8.45	12.71	52.1	0.29	1.22	0.91	8.09	1.50	8.99	1.02	11.52	1.5	139.7	12.4
1	1	4.8	2.3	3.71	15.2	0.25	1.13	0.19	2.05	1.38	2.24	1.08	4.70	2	176.6	40.5
1	2	8.9	4.35	6.71	27.5	0.27	1.19	0.43	4.06	1.46	4.49	1.04	6.99	2	182.6	27.3
1	4	17.1	8.45	12.71	52.1	0.29	1.22	0.91	8.09	1.50	8.99	1.02	11.52	2	186.3	16.5
0.5	1	1.0	0.4	3.71	3.8	0.25	0.20	0.19	0.06	0.44	0.26	1.08	1.78	1	88.3	53.6
0.5	2	2.1	0.91	6.71	6.9	0.27	0.25	0.43	0.18	0.52	0.61	1.04	2.17	1	91.3	43.9
0.5	4	4.1	1.94	12.71	13.0	0.29	0.28	0.91	0.42	0.57	1.33	1.02	2.92	1	93.1	32.6
0.5	1	1.0	0.4	3.71	3.8	0.25	0.20	0.19	0.06	0.44	0.26	1.08	1.78	1.5	132.5	80.4
0.5	2	2.1	0.91	6.71	6.9	0.27	0.25	0.43	0.18	0.52	0.61	1.04	2.17	1.5	136.9	65.8
0.5	4	4.1	1.94	12.71	13.0	0.29	0.28	0.91	0.42	0.57	1.33	1.02	2.92	1.5	139.7	48.9
0.5	1	1.0	0.4	3.71	3.8	0.25	0.20	0.19	0.06	0.44	0.26	1.08	1.78	2	17[illegible].6	107.2
0.5	2	2.1	0.91	6.71	6.9	0.27	0.25	0.43	0.18	0.52	0.61	1.04	2.17	2	1[illegible].6	87.7
0.5	4	4.1	1.94	12.71	13.0	0.29	0.28	0.91	0.42	0.57	1.33	1.02	2.92	2	1[illegible].3	65.2
2	1	20.0	9.9	3.71	60.8	0.25	4.89	0.19	38.05	5.13	38.24	1.08	44.45	1	88.3	2.1
2	2	36.4	18.1	6.71	110.0	0.27	4.94	0.43	70.31	5.21	70.74	1.04	77.00	1	91.3	1.2
2	4	69.2	34.5	12.71	208.4	0.29	4.97	0.91	134.86	5.26	135.77	1.02	142.04	1	93.1	0.7
2	1	20.0	9.9	3.71	60.8	0.25	4.89	0.19	38.05	5.13	38.24	1.08	44.45	1.5	132.5	3.2
2	2	36.4	18.1	6.71	110.0	0.27	4.94	0.43	70.31	5.21	70.74	1.04	77.00	1.5	136.9	1.9
2	4	69.2	34.5	12.71	208.4	0.29	4.97	0.91	134.86	5.26	135.77	1.02	142.04	1.5	139.7	1.0
2	1	20.0	9.9	3.71	60.8	0.25	4.89	0.19	38.05	5.13	38.24	1.08	44.45	2	176.6	4.3
2	2	36.4	18.1	6.71	110.0	0.27	4.94	0.43	70.31	5.21	70.74	1.04	77.00	2	182.6	2.5
2	4	69.2	34.5	12.71	208.4	0.29	4.97	0.91	134.86	5.26	135.77	1.02	142.04	2	186.3	1.3

Parameters from 0.25u TSMC process

u	3.74E+10	1/(V*sec)
2*lambda	0.25	u
hsw	0.61	none
hbot	0.32	none
'up	4.1	

Lossy Integrator

Note: Process parameters may be a little optimistic but relative performance should be as predicted.

File:lossy-integrator-speed-comp

K	W2	W1	SWn	SWp	BOTn	BOTp	SW comp Total	Bot comp Total	Load comp	Den	VEB1	Io,no dif GHz	Io GHz
P-channel Load, Conventional Layout													
1	0.75	0.73	1.24	1.25	0.96	0.98	2.49	1.94	2.03	6.45	1	40.8	12.8
2	1.50	1.46	0.92	0.94	0.96	0.98	1.86	1.94	2.03	5.83	1	40.8	14.2
4	3.00	2.93	0.77	0.78	0.96	0.98	1.55	1.94	2.03	5.52	1	40.8	15.0
1	0.75	0.73	1.24	1.25	0.96	0.98	2.49	1.94	2.03	6.45	1.5	61.1	19.2
2	1.50	1.46	0.92	0.94	0.96	0.98	1.86	1.94	2.03	5.83	1.5	61.1	21.2
4	3.00	2.93	0.77	0.78	0.96	0.98	1.55	1.94	2.03	5.52	1.5	61.1	22.4
1	0.75	0.73	1.24	1.25	0.96	0.98	2.49	1.94	2.03	6.45	2	81.5	25.6
2	1.50	1.46	0.92	0.94	0.96	0.98	1.86	1.94	2.03	5.83	2	81.5	28.3
4	3.00	2.93	0.77	0.78	0.96	0.98	1.55	1.94	2.03	5.52	2	81.5	29.9
P-channel Load, Concentric Layout													
1	3.80	3.71	0.25	0.254	0.194	0.206	0.50	0.40	2.18	3.08	1	37.8	26.7
2	6.87	6.71	0.27	0.28	0.429	0.454	0.55	0.88	2.11	3.55	1	39.1	23.3
4	13.02	12.71	0.29	0.296	0.907	0.955	0.58	1.86	2.07	4.52	1	39.8	18.3
1	3.80	3.71	0.25	0.254	0.194	0.206	0.50	0.40	2.18	3.08	1.5	56.7	40.1
2	6.87	6.71	0.27	0.28	0.429	0.454	0.55	0.88	2.11	3.55	1.5	58.6	34.9
4	13.02	12.71	0.29	0.296	0.907	0.955	0.58	1.86	2.07	4.52	1.5	59.8	27.4
1	3.80	3.71	0.25	0.254	0.194	0.206	0.50	0.40	2.18	3.08	2	75.6	53.5
2	6.87	6.71	0.27	0.28	0.429	0.454	0.55	0.88	2.11	3.55	2	78.1	46.5
4	13.02	12.71	0.29	0.296	0.907	0.955	0.58	1.86	2.07	4.52	2	79.7	36.5
N-Channel Load, Simple Layout													
1	0.75	3.00					0.76	0.72	1.25	2.73	1	66.0	30.2
2	1.50	6.00					0.69	0.72	1.25	2.66	1	66.0	31.1
4	3.00	12.00					0.65	0.72	1.25	2.62	1	66.0	31.5
1	0.75	3.00					0.76	0.72	1.25	2.73	1.5	99.0	45.3
2	1.50	6.00					0.69	0.72	1.25	2.66	1.5	99.0	46.6
4	3.00	12.00					0.65	0.72	1.25	2.62	1.5	99.0	47.3
1	0.75	3.00					0.76	0.72	1.25	2.73	2	132.0	60.4
2	1.50	6.00					0.69	0.72	1.25	2.66	2	132.0	62.1
4	3.00	12.00					0.65	0.72	1.25	2.62	2	132.0	63.0
N-Channel Load, Concentric Layout													
1	3.71	14.83					0.31	0.24	1.35	1.90	1	61.2	43.4
2	6.71	26.83					0.34	0.54	1.30	2.18	1	63.3	37.8
4	12.71	50.83					0.36	1.13	1.28	2.77	1	64.5	29.8
1	3.71	14.83					0.31	0.24	1.35	1.90	1.5	91.8	65.1
2	6.71	26.83					0.34	0.54	1.30	2.18	1.5	94.9	56.7
4	12.71	50.83					0.36	1.13	1.28	2.77	1.5	96.8	44.7
1	3.71	14.83					0.31	0.24	1.35	1.90	2	122.4	86.9
2	6.71	26.83					0.34	0.54	1.30	2.18	2	126.5	75.6
4	12.71	50.83					0.36	1.13	1.28	2.77	2	129.1	59.5

Stay Safe and Stay Healthy !

End of Lecture 35